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Embedded Controlled STATCOM with Thirty Bus System to Improve Power Quality

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Abstract:
The power transfer capability can be Increased by using FACTS devices in electrical distributed systems. Among all the FACTS devices the STATCOM is more efficient. STATCOM is a shunt connected device and it improves the system voltage stability by exchange the reactive power to the system. In this paper deals with power quality improvement in thirty bus system using embedded controlled STATCOM. Thirty bus system is modeled by using SIMULINK elements and is employed for simulation studies. The simulation results of thirty bus system with and without STATCOM are presented. The embedded controlled STATCOM is employed and tested in laboratory. The power quality is improved by adding the STATCOM in the existing network and also voltage stability is improved.

Keywords:- Voltage source converter (VSC), Distribution Static Synchronous Compensator, Thirty Bus System, Power Quality (PQ), FACTS, Embedded Controlled STATCOM.

I. INTRODUCTION

D-STATCOM is the most essential controller for distribution networks, It has been broadly used since 1990's to specifically regulate system voltage, improve voltage profile, reduce voltage harmonics, reduce transient voltage disturbances and load compensation. Rather than usually conventional capacitors and inductors combined with fast switches, the D-STATCOM uses a power electronics converter to produce the reactive power output. A STATCOM converter is controlled using PWM or voltage / current determining techniques. D-STATCOMs are used more often than STATCOM controllers. Compared to STATCOM, D-STATCOM have significantly lower rated power and in consequence, faster power electronics switches, thus the PWM carries frequency used in a distribution controller can be much higher than in a FACTS controller. It has a substantial positive impact on the dynamics of the D-STATCOM.

II. OPERATING PRINCIPLE OF D-STATCOM

The essential STATCOM model consists of a voltage source inverter, DC side Capacitors (C) with voltage V_{dc} on each capacitor and a coupling reactor (LC) or a transformer. The AC voltage difference across the coupling reactor produces reactive power exchange between the STATCOM and the power systems at the Point of Common Coupling (PCC). If the output voltage of the STATCOM (V_C) is more than the system Voltage (V_L) then reactive power is supplied to the power system and reverses happen if V_C is less than that of VL. The output voltage of the STATCOM can be controlled in two ways either by changing the switching angles while maintaining the dc capacitor voltage at a constant level or by changing DC capacitor voltage at fixed switching angles.. The configuration of the STATCOM is shown in Figure. 2.1.

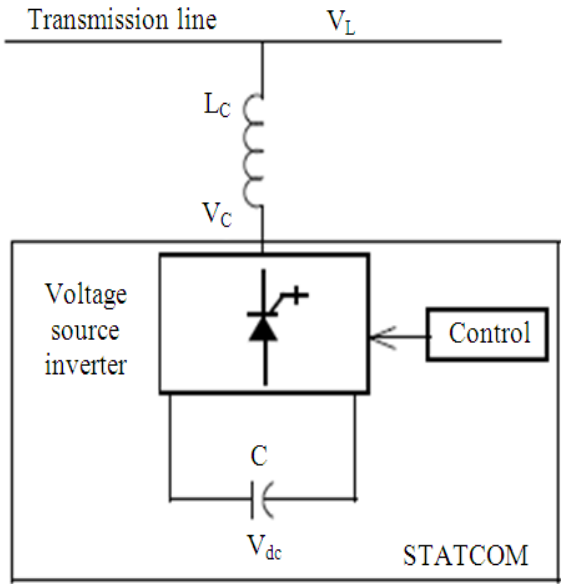


Figure .1 Configuration of the D-STATCOM

III. CASCADE MULTILEVEL INVERTER

The Cascade multilevel inverter consists of a number of H-bridge inverter units with separate DC source for each unit and is connected in cascade or series. In Figure. 2 two H-bridges (H1 and H2) are connected in cascade or series producing output voltage as shown in Figure 3.2. Each H-bridge can produce three different voltage levels: +Vdc, 0 and-Vdc by connecting the dc source to ac output side by different combinations of the four switches. The ac output of each H-bridge is connected in series such that the synthesized output voltage waveform is the sum of all of the individual H-bridge outputs By connecting the sufficient number of H-bridges in cascade and using proper modulation scheme, a nearly sinusoidal output voltage waveform can be synthesized. The number of levels in the output phase voltage is 2s+1, where s is the number of H-bridges used per phase. The Fig. 2b shows five-level output phase voltage waveform using two H-bridges. The switching angles α1 and α2 are corresponding to H1 and H2 respectively while β1 = π-α1 and β2 = π-α2. In case of 11-level CMLI five H-bridges per phase are required and the magnitude of the ac output phase voltage is given by sum of output voltages due to each H-bridge.

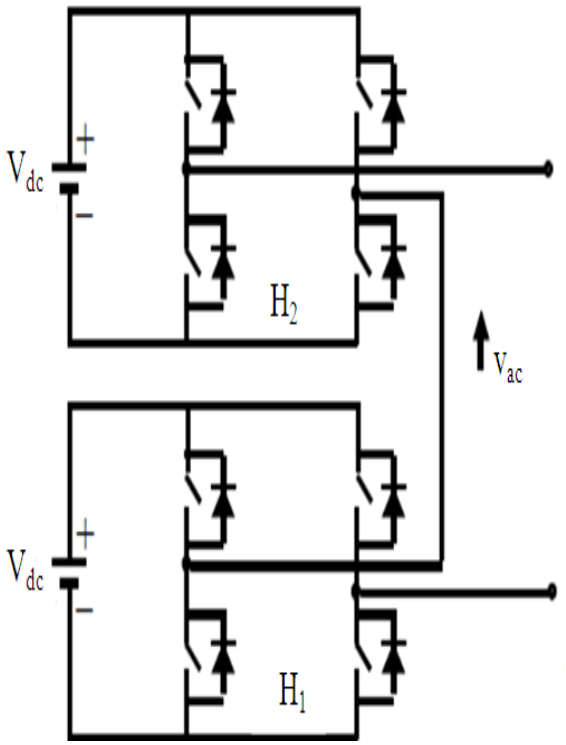


Figure 2. Configuration of five level cascaded multilevel inverter

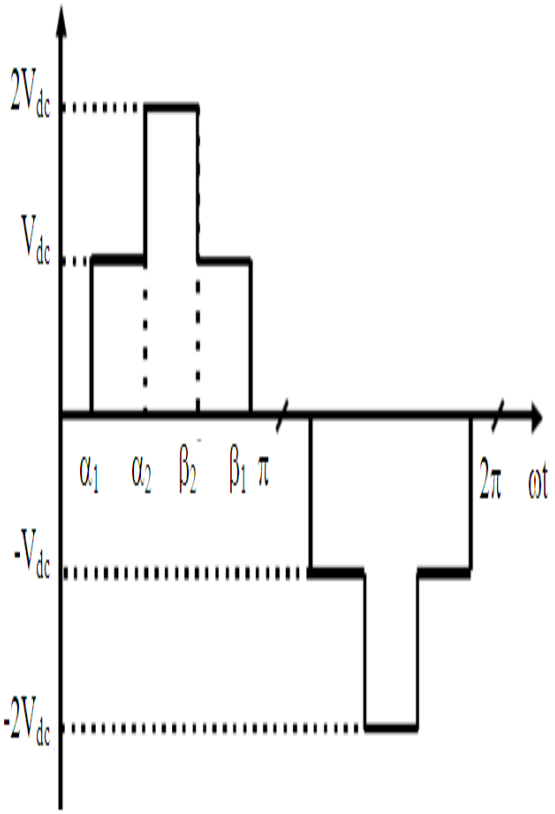


Figure 3 Output voltage of five level cascaded Multilevel inverter

IV. SELECTION OF SWITCHING ANGLE

To make multilevel AC output voltage using different levels of DC inputs, the semiconductor devices must be switched on and off in such a way that desired fundamental voltage obtained is nearly sinusoidal i.e., having minimum harmonic distortions. Different switching techniques are available for computing switching angles for the semiconductor devices (Kumar, 2003). Generally, the fundamental frequency switching scheme is considered more suitable for power system applications. In fundamental frequency switching scheme the devices are turned on and off once in a cycle, thereby producing less switching losses. Generally, the switching angles at fundamental frequency are computed by solving a set of nonlinear equations known as Selective Harmonic Elimination (SHE) equations such that certain order harmonic components (generally lower order) are eliminated Alternatively, the switching angles can be calculated by using some optimization based technique so that Total Harmonic Distortion (THD) up to certain order (generally up to 49th order) is minimized instead of eliminating some individual harmonic components.

V. EXPERIMENTAL RESULTS

Experimental setup of D-STATCOM is constructed and is shown in Figure 4(a). In D-STATCOM power circuit, IGBTs are used to create Five-level cascade inverter. This inverter is connected to AC grid by a three-phase coupling inductance. Gate pulses for the inverter are generated using PIC. Experimental setup consisting of controlling circuit and power circuit. PIC microcontroller is used for generating pulses. Two H-bridge inverters are used to get sinusoidal output with minimal harmonics. The rectifier voltage is shown in Figure 4(b) Switching pulse for M1 and M5 are sown in Figure (c). inverter output voltage is sown in Figure 4(d). The harmonic contents in the inverter output voltage can be reduced. This concept can be extended to 64 bus system.

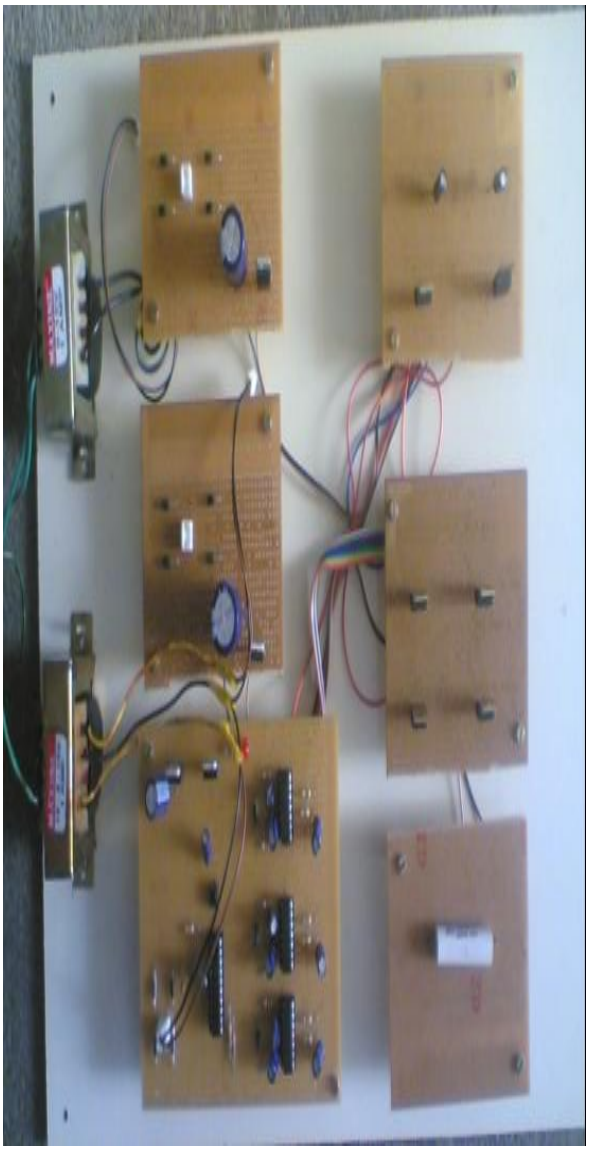
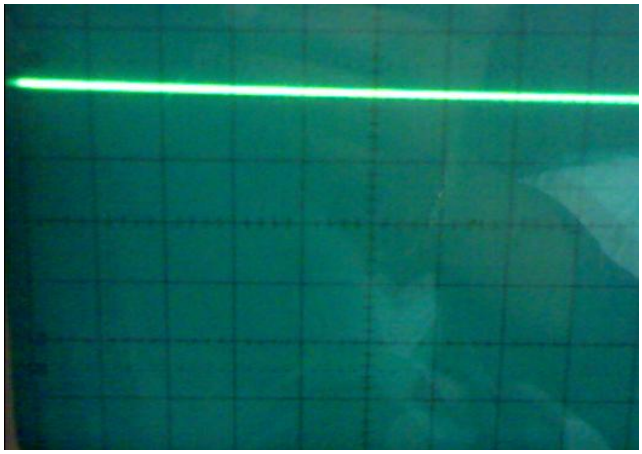
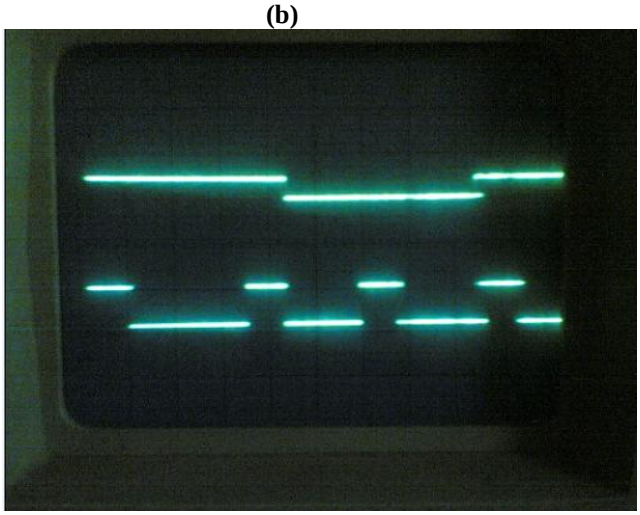


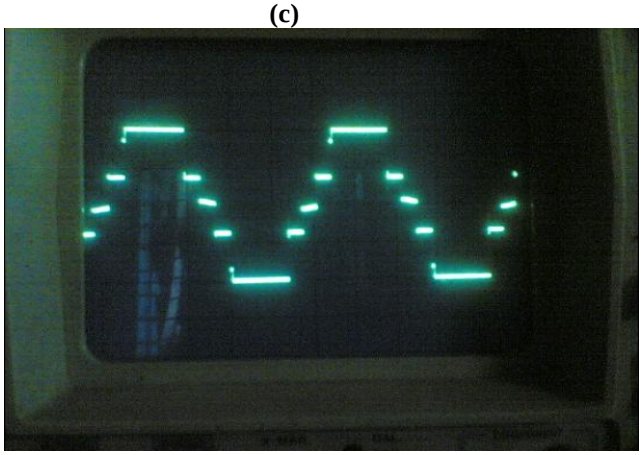
Figure (a)



(b)



(c)



(d)

Figure 41(a) Hardware snap shot 5 Level Inverter, (b) output voltage of rectifier,(c) Switching pulses for M1 & M5, (d) Output voltage of Inverter

Table 1. Real and reactive powers with and without VSI fed STATCOM

	Real power(MW)	Reactive power(MVAR)
Without STATCOM	**0.497**	**1.556**
With STATCOM	**0.853**	**2.869**

VI. SIMULATION RESULTS

The 30 bus system is considered for simulation studies. The circuit model of 30 bus system without D-STATCOM is shown in Figure 5. Each line is represented by series impedance model. The shunt capacitance of the line is neglected. The additional load is connected in parallel with the load 1. The voltage sag is appeared due to increased voltage drop or The voltage decreases due to the addition of the load. The reactive power (Q) at busses 4, 17 and 25 are shown in Figure 5(a),(b),(c).

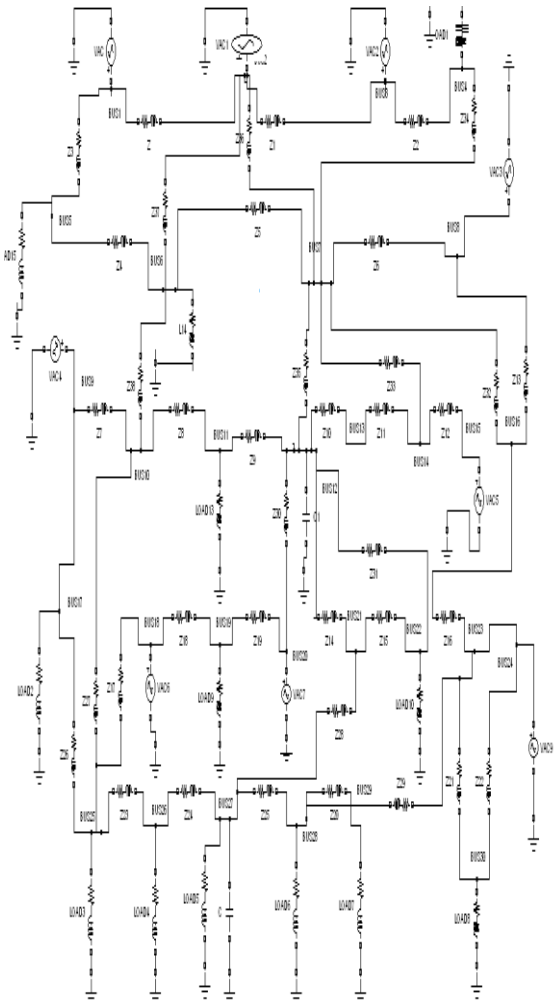


Figure 5: 30 bus system without D-STATCOM

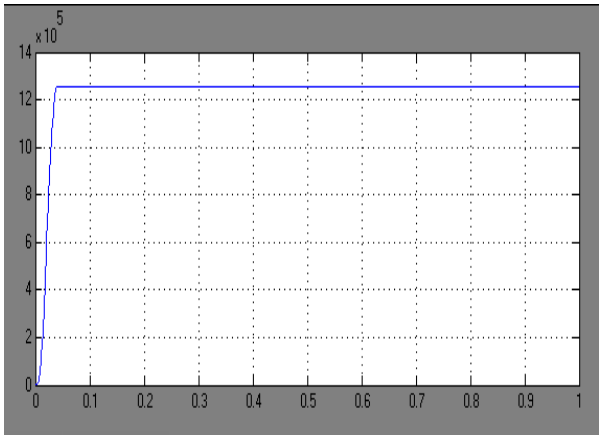


Figure 5(a): Reactive power at bus 4

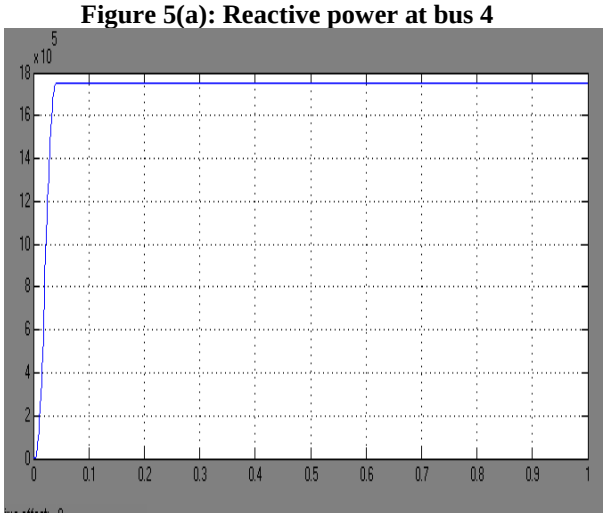


Figure 5(b): Reactive power at bus 17

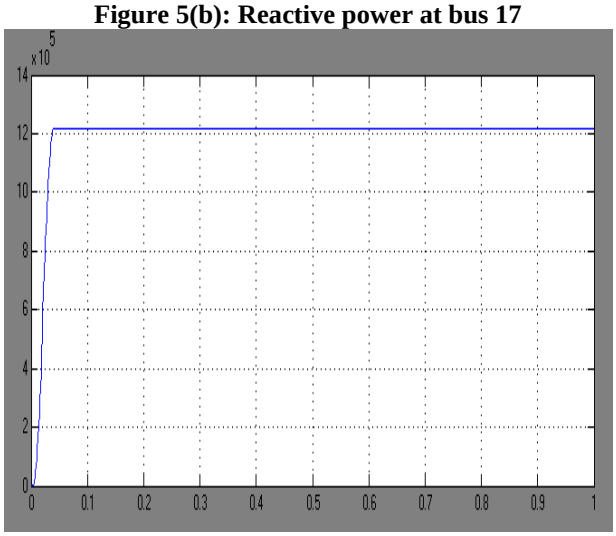


Figure 5(c): Reactive power at bus 25

Thirty bus system with D-STATCOM is shown in Figure6. The D-STATCOM is added to the bus 29 to improve power quality. The reactive power

of the loads connected to the nearby buses is studied. The reactive power in the buses 4, 17 and 25 are shown in Figures. 6.2a, 6.2b, and 6.2c respectively. The summary of the reactive power in various buses is given in Table 2. It can be seen that the reactive power increases in the buses near the D-STATCOM. The increase in reactive power is due to increase in the voltage of the nearby buses.

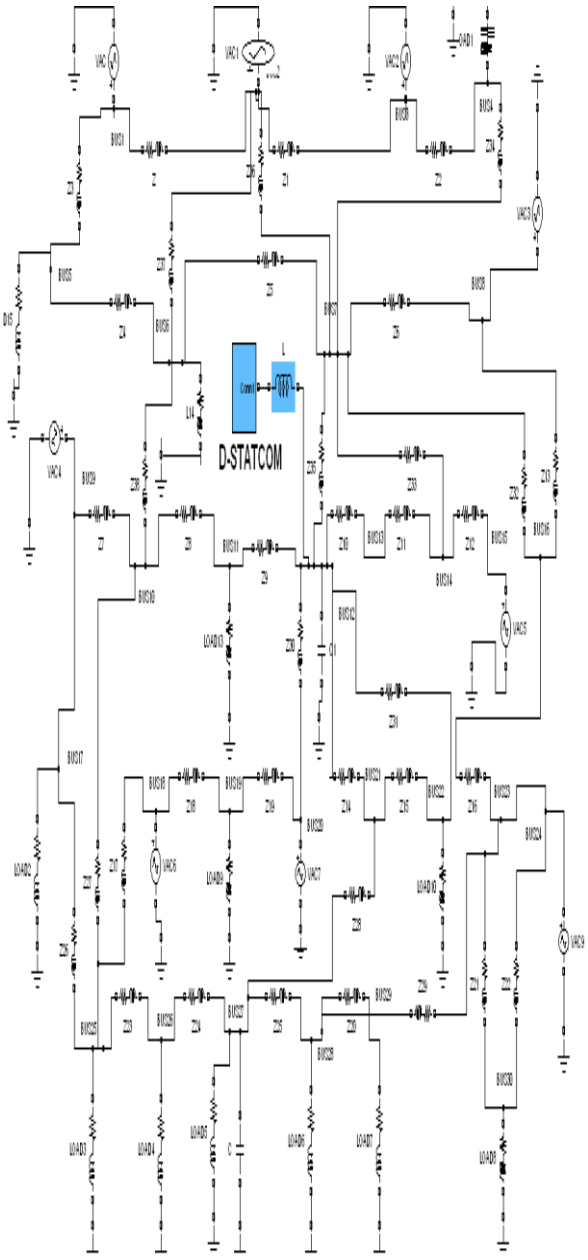


Figure 6: 30 bus system with D-STATCOM

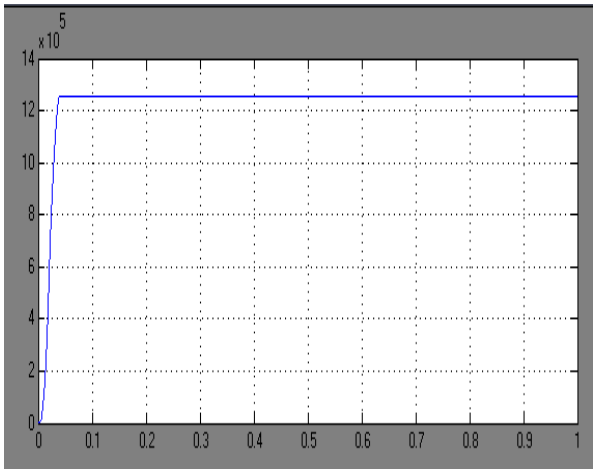


Figure 6(a): Reactive power at bus 4

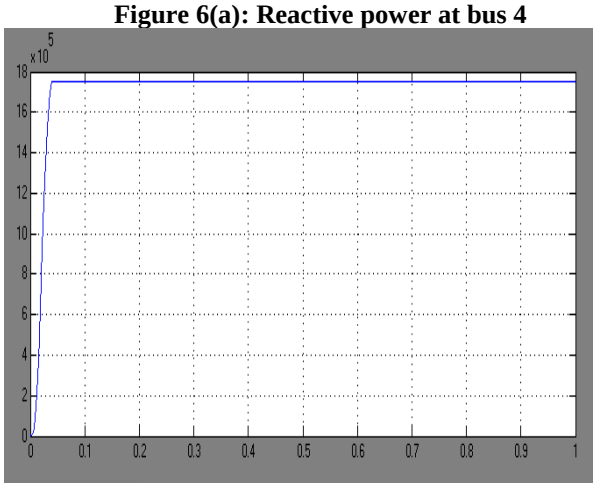


Figure 6(b): Reactive power at bus 17

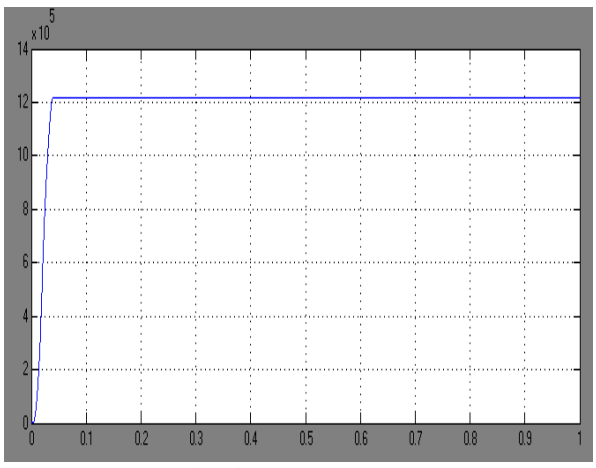


Figure 6(c): Reactive power at bus 25

Table 2: Summary of reactive Power (Q)

Bus no	Reactive power without D-STATCOM MVAR	Reactive power with D-STATCOM MVAR
Bus-4	1.256	1.257
Bus-5	1.136	1.139
Bus-11	1.065	1.072
Bus-17	1.745	1.749
Bus-19	1.323	1.343
Bus-22	1.343	1.027
Bus-25	1.018	1.218
Bus-27	1.217	1.102
Bus-30	0.933	0.974

VII. CONCLUSION

The power quality improvement in thirty bus system is increased by using embedded controlled STATCOM. Upon sequence of experiments in the laboratory it is proved that The Embedded controlled STATCOM with Thirty bus system is is achieved its objective in simulation with MATLAB SIMULINK.. The simulation results of with and without D-STATCOM are presented and the Voltage stability is also improved. This system has improved reliability and power quality. The simulation results are in line with the predictions. This concept can be extended to 50 bus system. We found few issues while integration and deployment of simulation of ingredients.

REFERENCES

[1] I. Papic, "Power Quality improvement using distribution staticcompensator with energy storage system," Proceedings of 9thInternational Conference on Harmonicsand. Quality Power, pp.916–920, 2000.

[2] O. A. Lara and E. Acha, "Modeling and analysis of custompower systems by PSCAD/EMTDC," IEEE Transactions onPower Delivery, vol. 17, no. 1, pp. 266- 272, 2002.

[3] M. K. Mishra, A. Ghosh and A. Joshi, "Operation of aDSTATCOM in voltage control mode," IEEE Transactions on Power Delivery, vol. 18, no. 1, 2003. [4] IEEE Recommended Practices and Requirements for Harmonics Fig. 7 Load current and the harmonic spectrum Control in Electric Power Systems, IEEE Std. 519, 1992.

[5] H. Akagi, E H Watanabe and M Aredes, Instantaneous powertheory and applications to power conditioning, John Wiley & Sons,New Jersey, USA, 2007.

[6] H. Fugita and H. Akagi, "Voltage-regulation performance of a shunt active filter intended for installation on a power distribution system," IEEE Trans. on Power Electron., vol. 22, no.1, pp. 1046-1053, May 2007.

[7] C. Schauder et al., "AEP UPFC project: Installation, commissioning and operation of the -160MVA STATCOM (Phase I)," IEEE Transactions on Power Delivery, vol.13, pp. 1530–1535, Oct. 1998.

[8] T. Zaveri, B. Bhavesh, N. Zaveri, "Control Techniques for Power Quality Improvement in Delta Connected Load Using DSTATCOM", IEEE International Electric Machines & Drives Conference (IEMDC), pp. 1397-1402, 2011.

[9] H. Hosseini, B. Tusi, N. Razmjooy, M. Khalilpoor, "Optimum Design of PSS and SVC Controller for Damping Low Frequency Oscillation (LFO)", Iranian Society of Instrumentation & Control Engineers, 2011.

[10] S.B. Karanki, N. Geddada, M.K. Mishra, B.K. Kumar, "A DSTATCOM Topology With Reduced DCLinkVoltage Rating for Load Compensation with Nonstiff Source", IEEE Transactions on Power Electronics, Vol. 27, No. 3, pp. 1201-1211, March 2012.